AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in this application.

LISTING OF THE CLAIMS:

Claim 1 (Original): A tuning circuit comprising:

a first reactance,

a second reactance, and

an insulated gate field effect transistor having a gate arranged to receive a control signal, the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first reactance and being connected between the drain of the field effect transistor and a second node,

wherein the first and second nodes are arranged so as to experience a balanced ac signal.

Claim 2 (Original): A circuit according to claim 1, wherein the first and second reactances are capacitors.

Claim 3 (Original): A circuit according to claim 1, wherein the first and second reactances are inductors.

Claim 4 (Original): A circuit according to claim 1, including a capacitor connected between said nodes.

Claim 5 (Original): A circuit according to claim 1, including an inductor connected between said nodes.

Claims 6-13 (Canceled)

Claim 14 (Original): A tuning circuit comprising:

a first reactance,

a second reactance, and

an insulated gate field effect transistor having a gate arranged to receive a control signal,

the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first reactance and being connected between the drain of the field effect transistor and a second node,

wherein

the first and second nodes are arranged so as to experience a balanced ac signal, and

the insulated gate field effect transistor comprises source and drain regions within a surrounding region and gate electrode means provided over a channel or channels between said source and drain regions and over at least part of the boundary between said source and drain regions and said surrounding region, said surrounding region being provided with ground connection means for connection to an AC ground.

Claim 15 (Original): A tuning circuit according to claim 14, wherein said ground connection means comprises a plurality of interconnected ohmic contacts to said surrounding region.

Claim 16 (Original): A tuning circuit according to claim 14, wherein said gate electrode means encompasses said source and drain regions.

Claim 17 (Original): A tuning circuit according to claim 14, wherein said source and drain regions are in a finger structure arrangement.

Claim 18 (Original): A tuning circuit according to claim 14, wherein said source and drain regions are in a waffle structure arrangement.

Claim 19 (Original): A tuning circuit according to claim 14, including a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductor or conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths.

Claim 20 (Original): A tuning circuit according to claim 19, wherein said source and drain regions are in a waffle structure arrangement.

Claim 21 (Original): A tuning circuit according to claim 20, wherein the interconnection layer comprises a source interconnection structure and a drain

interconnection structure, said structures comprising respective sets of fingers extending diagonally, with respect to said waffle structure arrangement, which are interdigitated.

Claim 22 (Original): A tuning circuit according to claim 14, wherein the first and second reactances are capacitors.

Claim 23 (Original): A tuning circuit according to claim 14, wherein the first and second reactances are inductors.

Claim 24 (Original): A tuning circuit according to claim 14, including a capacitor connected between said nodes.

Claim 25 (Original): A tuning circuit according to claim 14, including an inductor connected between said nodes.

Claim 26 (Original): A resonant circuit including a tuning circuit, the tuning circuit comprising:

a first reactance,

a second reactance, and

an insulated gate field effect transistor having a gate arranged to receive a control signal,

the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first

reactance and being connected between the drain of the field effect transistor and a second node,

wherein

the first and second nodes are arranged so as to experience a balanced ac signal, and

the insulated gate field effect transistor comprises source and drain regions within a surrounding region and gate electrode means provided over a channel or channels between said source and drain regions and over at least part of the boundary between said source and drain regions and said surrounding region, said surrounding region being provided with ground connection means for connection to an AC ground.

Claim 27 (Original): A resonant circuit according to claim 26, wherein said ground connection means comprises a plurality of interconnected ohmic contacts to said surrounding region.

Claim 28 (Original): A resonant circuit according to claim 26, wherein said gate electrode means encompasses said source and drain regions.

Claim 29 (Original): A resonant circuit according to claim 26, wherein said source and drain regions are in a finger structure arrangement.

Claim 30 (Original): A resonant circuit according to claim 26, wherein said source and drain regions are in a waffle structure arrangement.

Claim 31 (Original): A resonant circuit according to claim 26, including a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductor or conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths.

Claim 32 (Original): A resonant circuit according to claim 31, wherein said source and drain regions are in a waffle structure arrangement.

Claim 33 (Original): A resonant circuit according to claim 32, wherein the interconnection layer comprises a source interconnection structure and a drain interconnection structure, said structures comprising respective sets of fingers extending diagonally, with respect to said waffle structure arrangement, which are interdigitated.

Claim 34 (Original): A resonant circuit according to claim 26, wherein the first and second reactances are capacitors.

Claim 35 (Original): A resonant circuit according to claim 26, wherein the first and second reactances are inductors.

Claim 36 (Original): A resonant circuit according to claim 26, including a capacitor connected between said nodes.

Claim 37 (Original): A resonant circuit according to claim 26, including an inductor connected between said nodes.

Claim 38 (Original): A resonant circuit according to claim 26, comprising an oscillator.

Claim 39 (Original): A resonant circuit according to claim 26, comprising a filter.

Claim 40-42 (Canceled)